

## **AMENDMENTS TO THE CLAIMS**

The following listing of claims will replace all prior versions and listings of claims in the application.

### **LISTING OF CLAIMS**

1. (original) A voltage-controlled oscillator, comprising:

a voltage-controlled phase-shift circuit, outputting an output signal with a phase of an input signal shifted by a specified amount according to an external control voltage;

a SAW resonator, resonating at a specified resonance frequency, and;

a buffer, inputting a signal from the SAW resonator and outputting the signal as a clock signal with a specified frequency; and outputting an output signal for a positive-feedback oscillation loop,

wherein the voltage-control phase-shift circuit, the SAW resonator, and the buffer form the positive-feedback oscillation loop, and a frequency temperature characteristic of the SAW resonator is corrected by rotating the frequency temperature characteristic of the SAW resonator by a specified amount using a temperature characteristic of propagation delay time of the buffer.

2. (currently amended) The voltage-controlled oscillator according to Claim

1, wherein the buffer further comprises:

\_\_\_\_\_ ~~includes~~ a first differential amplifier, amplifying a signal from the SAW resonator and outputting the signal;

\_\_\_\_\_a second differential amplifier, inputting the signal outputted from the first differential amplifier, of which either one of a non-inversion output terminal and an inversion output terminal outputs the positive-feedback-oscillation-loop output signal;  
and  
\_\_\_\_\_a third differential amplifier, inputting the signal from the first differential amplifier and outputting the signal as a clock signal with a specified frequency,  
\_\_\_\_\_wherein the propagation delay time of the buffer is a propagation delay time between the first differential amplifier and the second differential amplifier connected to the first differential amplifier.

3. (currently amended) The voltage-controlled oscillator according to Claim 2, wherein the differential amplifier further comprises a differential amplifier circuit using an ECL line receiver.

4. (currently amended) The voltage-controlled oscillator according to Claim 1, wherein the buffer further comprises:  
\_\_\_\_\_includes a first amplifier, amplifying a signal from the SAW resonator and outputting the signal;  
\_\_\_\_\_a second amplifier, inputting the signal outputted from the first amplifier and outputting the signal as the positive-feedback-oscillation-loop output signal; and  
\_\_\_\_\_at least one third amplifier, inputting the signal outputted from the first amplifier and outputting the signal as a clock signal with a specified frequency,

\_\_\_\_\_ wherein the propagation delay time is a propagation delay time between the first amplifier and the second amplifier connected to the first amplifier.

5. (currently amended) The voltage-controlled oscillator according to ~~one of~~ Claims 1 ~~to~~ 4, wherein the SAW resonator uses an in-plane rotated ST-cut quartz crystal plate with Euler angles of  $(0, 113^\circ \text{ to } 135^\circ, \pm(40^\circ \text{ to } 49^\circ))$ .

6. (currently amended) The voltage-controlled oscillator according to ~~one of~~ Claims 1 ~~to~~ 5, further comprising:

\_\_\_\_\_ an impedance circuit, generating a specified potential difference between the non-inversion input terminal and the inversion input terminal of the buffer; and

\_\_\_\_\_ an NTC thermistor having a negative temperature characteristic in parallel to the impedance circuit, between the non-inversion input terminal of the buffer and the terminal of the SAW resonator adjacent ~~at~~ the downstream end of the feedback loop.

7. (currently amended) A clock converter, forming a feedback loop constructed of a voltage-controlled oscillator, in which frequency varies depending on a supplied control voltage and which outputs a feedback-loop output signal, a phase comparing section, comparing phases of the feedback-loop output signal from the voltage-controlled oscillator and an external input signal to output a phase-difference signal, and a loop filter, smoothing a phase difference signal to generate the control voltage, wherein the voltage-controlled oscillator comprises:

\_\_\_\_\_ a voltage-controlled phase-shift circuit, outputting an output signal with the phase of an input signal shifted by a specified amount according to the control voltage;<sub>17</sub>

\_\_\_\_\_ a SAW resonator, resonating at a specified resonance frequency;<sub>17</sub> and

\_\_\_\_\_ a buffer, inputting a signal from the SAW resonator and outputting the signal as a clock signal with a specified frequency, and outputting an output signal for a positive-feedback oscillation loop and the feedback-loop output signal,

\_\_\_\_\_ wherein the voltage-controlled phase-shift circuit, the SAW resonator, and the buffer form a positive-feedback oscillation loop, and wherein a frequency temperature characteristic of the SAW resonator is corrected by rotating the frequency temperature characteristic of the SAW resonator by a specified amount using a temperature characteristic of propagation delay time of the buffer.

8. (currently amended) The clock converter according to Claim 7, wherein the buffer further comprises:

\_\_\_\_\_ ~~includes~~ a first differential amplifier, amplifying a signal from the SAW resonator and outputting the signal;<sub>17</sub>

\_\_\_\_\_ a second differential amplifier, inputting the signal outputted from the first differential amplifier, of which either one of a non-inversion output terminal and an inversion output terminal outputs the feedback-loop output signal and the other output terminal outputs the positive-feedback-oscillation-loop output signal;<sub>17</sub> and

\_\_\_\_\_ a third differential amplifier, inputting the signal from the first differential amplifier and outputting the signal as a clock signal with a specified frequency,

\_\_\_\_\_ wherein the propagation delay time of the buffer is a propagation delay time between the first differential amplifier and the second differential amplifier connected to the first differential amplifier.

9. (currently amended) The clock converter according to Claim 8, wherein the differential amplifier further comprises a differential amplifier circuit using an ECL line receiver.

10. (currently amended) The clock converter according to Claim 7, wherein the buffer further comprises:

\_\_\_\_\_ ~~includes~~ a first amplifier, amplifying a signal from the SAW resonator and outputting the signal;

\_\_\_\_\_ a second amplifier, inputting the signal outputted from the first amplifier and outputting the signal as an output signal for the positive-feedback oscillation loop; and

\_\_\_\_\_ a plurality of third amplifiers, inputting the signal outputted from the first amplifier, outputting at least one clock signal having a specified frequency, and outputting the feedback-loop output signal,

\_\_\_\_\_ wherein the propagation delay time is a propagation delay time between the first amplifier and the second amplifier connected to the first amplifier.

11. (currently amended) The clock converter according to ~~one of~~ Claims 7 to 10, wherein the SAW resonator uses an in-plane rotated ST-cut quartz crystal plate with Euler angles of (0, 113° to 135°,  $\pm(40^\circ$  to  $49^\circ)$ ).

12. (currently amended) The clock converter according to ~~one of Claims 7 to 11~~, further comprising:

\_\_\_\_\_an impedance circuit, generating a specified potential difference between a non-inversion input terminal and an inversion input terminal of the buffer; and

\_\_\_\_\_an NTC thermistor having a negative temperature characteristic in parallel to the impedance circuit, between the non-inversion input terminal of the buffer and the terminal of the SAW resonator adjacent ~~to the downstream~~ end of the feedback loop.

13. (currently amended) An electronic device, comprising a clock converter according to ~~one of Claims 7 to 12~~.